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A Digital Approach to Adaptive Delta Modulation

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A fixed-step-size delta modulator followed by digital circuits for generating an adaptive delta modulation signal provides an attractive compromise between code efficiency and cost. In order to control the total quantizing noise, the fixed-step-size delta modulation sampling rate is higher than the adaptive delta modulation output rate. Computer simulations, based on the adaptive delta modulation technique described by N. S. Jayant, indicate that the sampling rate required for negligible degradation relative to a conventional adaptive delta modulator is well within the current state of the art. Our approach lends itself to any scheme of step-size variation and may use any means of single-integration, fixed-step-size delta modulation.

I. INTRODUCTION

Since the invention of delta modulation, considerable effort has been devoted to devising means of improving code efficiency without sacrificing the inherent simplicity of the analog-to-digital converter. The key to success in this respect is the retention of a single binary decision for each sample of the analog input. Early work concentrated on sophisticated linear signal processing to be introduced either at the input to the delta modulator, as a predictor in the feedback loop, or as an error filter in the forward loop.[1–3] In recent years, the use of a time-varying step size in the feedback loop has been emphasized.[4–8] Although the step-size variation, in a sense, transforms the delta modulator from a binary to a multilevel device, implementation is likely to be more economical than that of a conventional multilevel quantizer. The variable-step-size, sometimes called "adaptive" or "companding," mechanism provides considerable improvement in efficiency and it is possible that for speech encoding, this form of

delta modulation will result in better performance characteristics in the 20–40 kilobit/second range than conventional PCM.

II. THE DIGITAL DELTA MODULATOR

The purpose of this paper is to present a new approach to the implementation of adaptive delta modulators. The approach is motivated by current trends in electronic device technology that suggest that digital hardware implementations based on standardized building blocks will offer advantages of economy and flexibility relative to analog techniques. This hypothesis combined with the observation that *transmission rate rather than analog-to-digital conversion rate* influences the overall cost of a digital communication system suggests the use of the very simple single-integration delta modulator for analog-to-digital conversion and digital hardware for converting the single-integration, fixed-step-size representation to the desired efficient format. By separating analog-to-digital conversion from source encoding, we obtain a compromise between the goals of economy of implementation and efficiency of representation. This compromise, based on the addition of only digital devices to the simple delta modulator, promises, in many situations, to be more economical than the conventional approach of performing analog-to-digital conversion and souree encoding in one step. This point of view has led to a new type of PCM encoder that combines a delta modulator with a nonrecursive digital filter.[9]

The digital circuits required to convert a simple delta modulation signal to a variable-step-size format comprise a "digital delta modulator" operating on the integrated output of the first delta modulator. In addition to a sequential cireuit that determines the appropriate step size at each instant, the digital delta modulator contains only binary counting and addition circuits and one simple decision element. Figure 1 is an operational block diagram of the entire eneoder.

III. PERFORMANCE CHARACTERISTICS

Computer simulations have verified the feasibility of the combination of a fixed-step-size delta modulator and a digital delta modulator. N. S. Jayant's scheme of adaptive delta modulation[6] was simulated by means of software provided by Jayant and Mrs. K. Shipley. For a given output rate, the operation of the digital delta modulator in Fig. 1 is determined completely by the step-size logic. At eaeh instant, the step size depends on the previous step size and the cur-

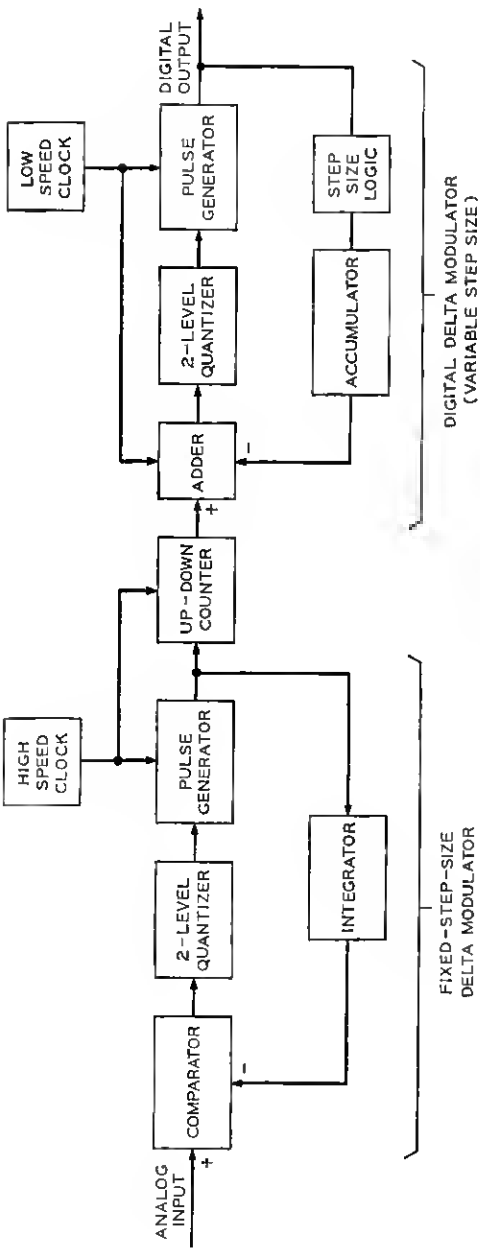

Fig. 1—Functional block diagram.

rent and previous binary outputs. If the binary outputs are identical, the current step size is 1.5 times the previous step size; if they differ, it is 0.66 times the previous step size. In addition to the output rate of the digital delta modulator, the design parameters in Fig. 1 are the step size and sampling rate of the fixed-step-size delta modulator. In our simulations, the product of step size and sampling rate, and thus the maximum slope of the delta modulator, was held constant. This constant was chosen on the basis of previous simulations by Jayant of fixed-step-size delta modulators operating on the speech tapes used in our simulations.

Our results are shown in Fig. 2 as curves of output signal-to-noise ratio (S/N) plotted against the sampling rate of the fixed-step-size delta modulator for two different output rates. It is not surprising that for low sampling rates of the first delta modulator, it is the error performance of this device that largely determines the overall S/N. As the sampling rate increases, the integrated output of the fixed-step-size delta modulator becomes arbitrarily close to the analog input and the asymptotic S/N is identical to that of an adaptive delta modulator operating directly on the analog input. (A separate simulation has verified this statement.) The simulation results are quite encouraging

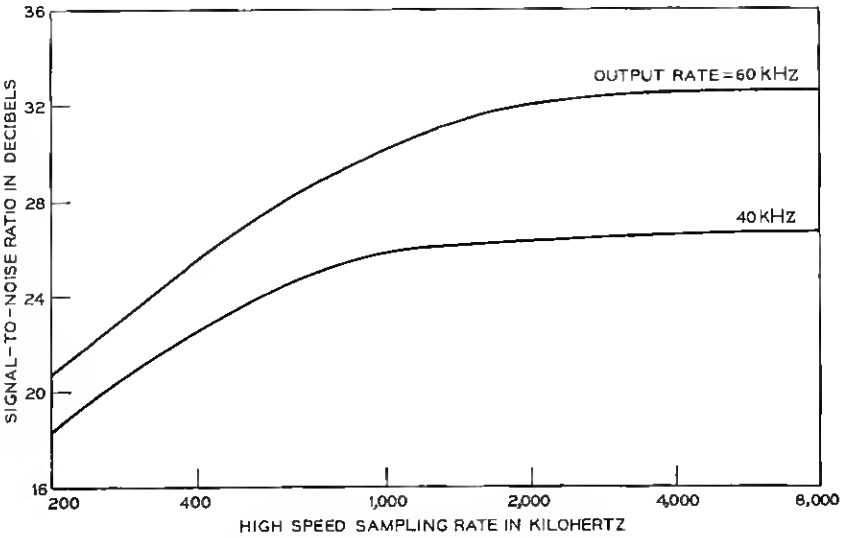

Fig. 2—Performance characteristics.

because they show that for the output rates considered, which are in the range of practical interest, the high-speed sampling rate required for negligible performance degradation relative to a conventional implementation is well within the state of the art.

By contrast with this empirical means of determining the rate and step size of the high-speed delta modulator, one may take the following conservative approach: (*i*) Set the step size at the minimum step size of the adaptive delta modulator, thus assuring that the quantizing resolution is not compromised and (*ii*) let the high-speed clock rate be the final output rate times the ratio of maximum to minimum step size so that the maximum slope is not reduced. A typical ratio of maximum to minimum step size is 128:1 so that with an output rate of 64 kb/s, the fixed-step-size delta modulator is required to operate at 8,192 kHz according to this conservative criterion.

IV. PRACTICAL IMPLEMENTATION

Figure 1 is a functional block diagram which indicates the required signal processing operations. In a hardware implementation, considerable simplification is possible. The up-down counter and the adder and accumulator of the digital delta modulator may be combined in a single accumulator as shown in Fig. 3. This accumulator is modified by +1 or −1 for each sample of the fixed-step-size delta modulator and it changes by the magnitude of the step size at each output sampling instant.

The two-level quantizer determines the polarity of each output pulse according to the state of a single bit of the accumulator. The step-size logic provides a digital representation of the current step size. Various means of providing this indication are possible, each appropriate to a different scheme of step-size variation. One method involves choosing the step size from a "dictionary" according to the output state of the adaptation logic. This technique lends itself to implementation by means of a "table-look-up" from a set of read-only memory registers, each containing one of the possible step sizes. Another technique is to specify the current step size as an arithmetic function of the previous step size—for example a multiple of or incremental change from the previous step size. For this type of adaption, the digital delta modulator could conveniently contain a step-size register which is arithmetically modified according to the output of the adaptation logic.

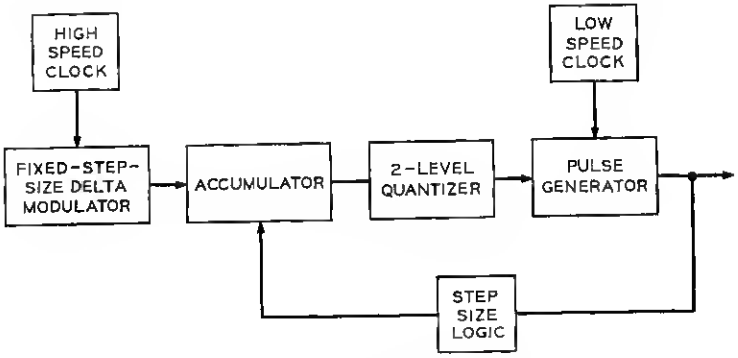

Fig. 3—Simplified implementation.

V. CONCLUSION

The technique described in this paper combines the simplicity of analog-to-digital conversion provided by fixed-step-size delta modulation with the code efficiency of variable-step-size delta modulation. Only a single step size need be precisely controlled with analog hardware; the step-size variation is controlled digitally, and is therefore exact. The technique lends itself to any scheme of step-size variation and any means of fixed-step-size, single-integration delta modulation.

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